

ABSTRACT OF THE DISCLOSURE

Whether a header information processor quickly enters a program inactive state at the timing when it issues an operation start command of an encoding
5 process for a predetermined processing unit to a variable-length code encoder, or the header information processor enters the program inactive state upon completion of execution steps to be processed is adaptively selected in accordance with the number of
10 execution steps. One memory is shared by the header information processor and variable-length code encoder, and address input permission means for controlling to grant permission of an address input to the memory to one of the header information processor and the
15 variable-length code encoder is provided. The memory is used as a work area of the header information processor, and as a storage area of a variable-length code table which is looked up by the variable-length code encoder.

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